ACS APPLIED MATERIALS & INTERFACES

Research Article

www.acsami.org

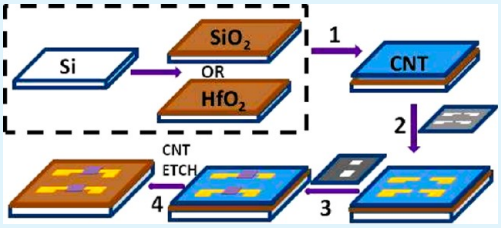
High-Performance Printed Carbon Nanotube Thin-Film Transistors Array Fabricated by a Nonlithography Technique Using Hafnium Oxide Passivation Layer and Mask

Suresh Kumar Raman Pillai and Mary B. Chan-Park*

School of Chemical and Biomedical Engineering, Nanyang Technological University, 62 Nanyang Drive, Singapore 637459

Supporting Information

ABSTRACT: The large-scale application of semiconducting single-walled carbon nanotubes (s-SWCNTs) for printed electronics requires scalable, repeateable, as well as noncontaminating assembly techniques. Previously explored nanotube deposition methods include serial methods such as inkjet printing and parallel methods such as spin-coating with photolithography. The serial methods are usually slow, whereas the photolithography-related parallel methods result in contamination of the nanotubes. In this paper, we report a reliable clean parallel method for fabrication of arrays of carbon nanotube-based field effect transistors (CNTFETs) involving shadow mask patterning of a passivating layer of Hafnium oxide (HfO_2) over the nanotube (CNT) active channel regions and plasma etching of the unprotected nanotubes. Pure (99%) semiconducting SWCNTs are first sprayed over the entire surface of a wafer substrate followed by a two-step shadow masking procedure to first deposit metal electrodes and then a HfO_2 isolation/passivation layer over the device channel region. The exposed SWCNT network outside the HfO_2 protected area is removed with oxygen plasma etching. The HfO_2 thus serves as both the device isolation mask during the plasma etching and as a protective passivating layer in subsequent use. The fabricated devices on SiO_2/Si substrate exhibit good device performance metrics, with on/off ratio ranging from 1×10^1 to 3×10^5 and mobilities of 4 to 23 $cm^2/(V\ s)$. The HfO_2/Si devices show excellent performance with on/off ratios of 1×10^2 to 2×10^4 and mobilities of 8 to 56 $cm^2/(V\ s)$. The optimum devices (on HfO_2/Si) have an on/off ratio of 1×10^4 and mobility as high as 46 $cm^2/(V\ s)$. This HfO_2-based patterning method enables large scale fabrication of CNTFETs with no resist residue or other contamination on the device channel. Further, shadow masking circumvents the need for expensive and area-limited lithography patterning process. The device channel is also protected from external environment by the HfO_2 film and the passivated device shows similar (or slightly improved) performance after 300 days of exposure to ambient conditions.



KEYWORDS: *carbon nanotube, thin film transistor, hafnium oxide, passivation, shadow mask patterning, electrical characteristics*

INTRODUCTION

The market for printed electronics is estimated to be about $300 B by 2017 (according to IDTechEx) but is currently lacking a high performance semiconductor. There are many applications for printed electronics including stretchable electronics,[1] conformable electronics,[2] sensors,[3] photovoltaics,[4] macroelectronics,[5] etc. Semiconducting single-walled carbon nanotubes (s-SWCNTs) are considered to be a highly promising semiconductor material for printed electronics to complement, and perhaps ultimately replace, conventional materials, e.g., amorphous Si or organic semiconductors, in complementary metal oxide semiconductor (CMOS) circuits.[6−13] SWCNT transistors have been shown to outperform conventional silicon transistors due to ballistic electronic transport, high intrinsic carrier mobility and lack of surface dangling bonds.[14,15] Earlier works by Beecher et al. demonstrated inkjet printing to fabricate unsorted SWCNT devices on Si substrates but the devices had low mobility (0.07 $cm^2/(V\ s)$) and on/off ratio of no more than 100.[16] Okimoto et al. fabricated inkjet printed (unsorted) SWCNT devices with mobility 1.6 to 4.2 $cm^2/(V\ s)$ and on/off ratio on the order of 1 $\times 10^4$ to 1×10^5.[17] With unsorted SWCNTs, the density of the nanotube network needs to be controlled to low values to achieve high switching. Recently, Sun et al. reported thin film SWCNT transistors on transparent substrates using a floating-catalyst chemical vapor deposition followed by gas phase filtration and a transfer process. They achieved mobility of 68 $cm^2/(V\ s)$ with an on/off ratio of 1×10^4 by controlling the network density to prevent metallic nanotube networks bridging the source and drain.[7] The large scale fabrication of carbon nanotube-based field-effect transistors (CNTFETs) remains challenging.

A first difficulty in CNTFET fabrication has been that all known SWCNT synthesis methods produce mixtures of nanotubes with different chiralities and metallicities. Metallic and semiconducting nanotubes are cosynthesized so that the as-synthesized products are unsuitable for use as the FET active channel material. To achieve homogeneous high-purity semi-

Received: October 22, 2012
Accepted: November 29, 2012
Published: November 29, 2012

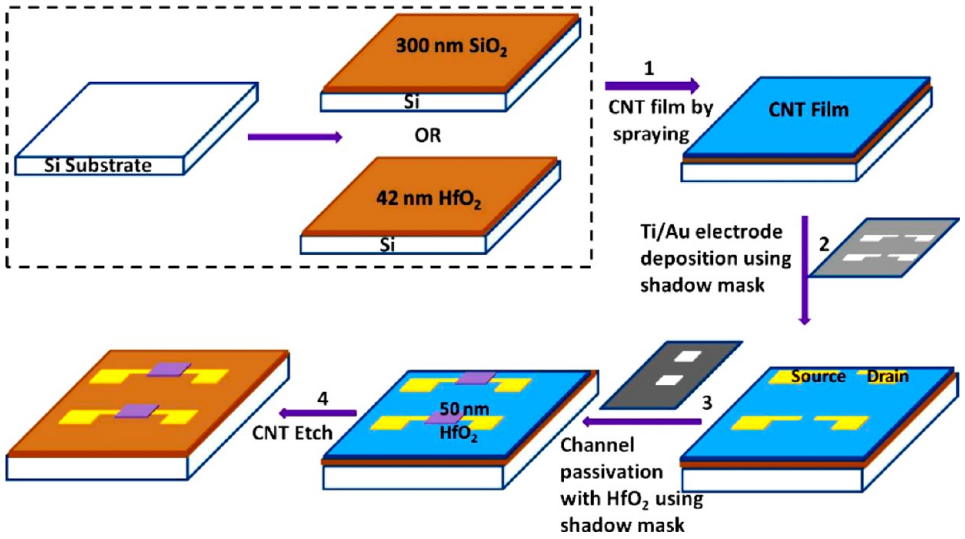


Figure 1. Schematic diagram of the fabrication procedure for CNTFET on HfO_2/Si or SiO_2/Si substrate using CNT spray deposition and channel passivation process. Step 1, deposition of CNT network film by spray process (blue color represents CNT film on substrate). Step 2, fabrication of S/D electrodes (yellow) using first shadow mask pattern. Step 3, E-beam deposition, through second shadow mask pattern, of 50 nm HfO_2 to cover CNT network on device channel. Step 4, etch of unprotected CNTs to isolate individual devices.

conducting samples, we must sort newly synthesized SWCNTs to separate the metallic (m-) nanotubes from the semiconducting (s-) species. The m-SWCNTs and s-SWCNTs are similar in many respects so that metallicity-based sorting has been challenging.[18,19] Some innovative technologies, such as density gradient ultracentrifugation (DGU), have recently been reported to achieve good SWCNT selectivity by electronic type, diameter and chirality but most involved solution processing of the nanotubes.[20−25] Printing, as opposed to direct growth, of SWCNT field-effect transistors (FETs) offers a device fabrication route to exploit the sorted semiconducting-enriched nanotubes (s-SWCNTs) as well as other solution processing advantages, such as simplicity and versatility, particularly room-temperature processing and the ability to employ large area, flexible, or transparent substrates.[6,26]

Recently, there has been great interest in the demonstration of high-performance transistors with sorted s-SWCNTs.[20] Miyata et al. fabricated CNTFETs by the simple drop coating method using long semiconducting nanotubes with less intertube junctions to achieve impressive mobility of 100 $cm^2/(V\ s)$ with on/off ratio of 1×10^5. They used an extra gel filtration step to obtain longer tubes although the additional filtration step would considerably reduce the yield of the purification process.[27] Ha et al. fabricated CNTFET devices and circuits on plastic substrate with ionic gel gate dielectric and used aerosol jet printing method to deposit the nanotubes and ion gel. The devices were ambipolar with hole and electron mobilities of ~20 $cm^2/(V\ s)$ with on/off ratio of 1×10^4.[28] However, the applicability of ion gel in long-term usable devices needs further testing and verification. Rouhi et al. reported s-SWCNT devices which have mobilities of 20 $cm^2/(V\ s)$ (actual values for 5 devices vary from ~5 to 40 $cm^2/(V\ s)$) with on/off ratio 1×10^4. They deposited the semienriched nanotube solution by drop-casting on the substrate prior to electrode deposition.[29,30] Controlling the network density is challenging by the solution dropping method so that there is significant scatter in the device performance.

A second difficulty in CNTFET fabrication has been a lack of fully satisfactory technology for large-scale production of reproducible FETs by solution processing of SWCNTs. Thus far, serial methods such as ink jet printing and drop casting, and parallel methods involving photolithography have been applied to sorted s-SWCNTs to fabricate transistors. Serial methods are time-consuming. The parallel methods commonly apply standard photolithography and etching patterning methods to isolate individual SWCNT-based devices from each other.[12,31] After device fabrication, the channel area is protected with photoresist and the unprotected SWCNTs in other areas are removed by plasma etching. Zhou and Bao have separately demonstrated superior FETs with separated s-SWCNTs with photolithography-based techniques.[12,32] However, photolithography has the drawback of reduction in CNT network density during resist removal and residual resist contamination of the SWCNTs in the active channel.[33] The residual resist on the SWCNTs likely degrades device performance. Also, photolithography is expensive and limited to the wafer size. It has recently been reported that the lack of reproducible large-scale assembly techniques for nanowires/nanotubes is still a major hurdle to their industrial application.[4] A cost-effective parallel patterning technique is still needed for the assembly of nanotube transistors for printed electronics.

A third consideration is that SWCNTs have very high surface area to volume ratio and perform better if they are passivated to minimize environment noise effects on the FET active channel. There are relatively few reports of nanotube device channel passivation.[34−37] The passivation materials investigated for back-gated CNT devices include HfO_2,[34] Si_3N_4,[35] Polymethyl methacrylate[36] and Parylene-C.[37] Previous passivation studies of CNT devices using HfO_2 and Si_3N_4 layers, deposited by atomic layer deposition and catalytic chemical vapor deposition respectively, found that the electrical characteristics of the CNT devices typically change from p-type to n-type. The vacuum processes remove the oxygen adsorbed on the nanotubes, thereby altering the interfacial charges. Device passivation with PMMA and Parylene-C have been attempted to try to reduce hysteresis. Recent studies on passivation of CNTFETs with hexamethyldisiloxane[38] show improved device-to-device uniformity and stability. However, none of the previous studies

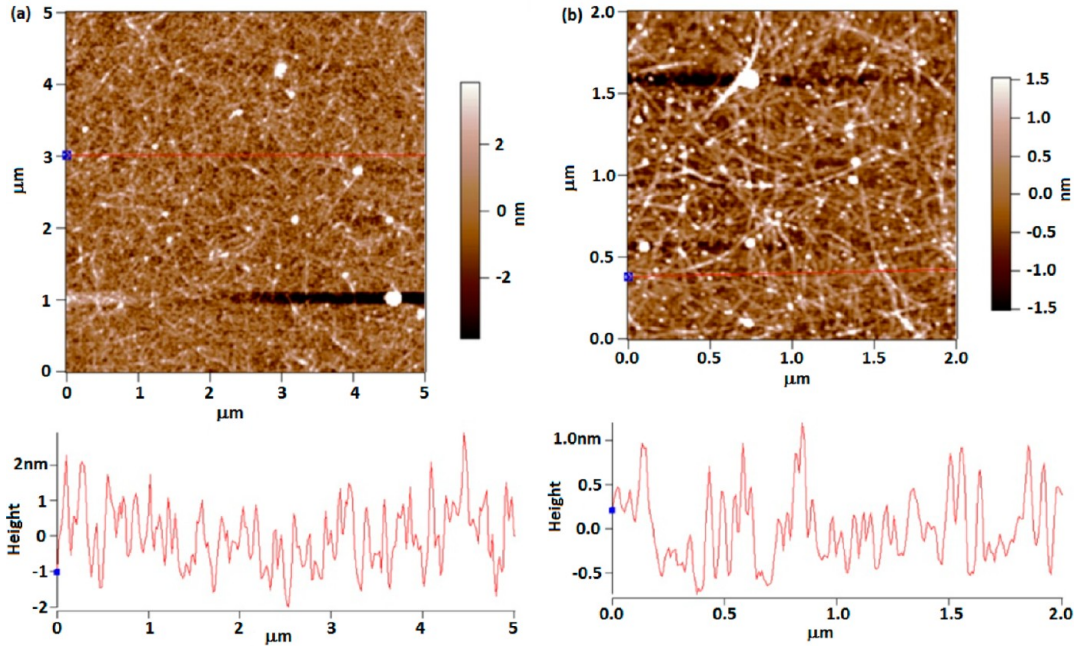


Figure 2. Representative AFM images of SWCNTs on (a) HfO_2/Si and (b) SiO_2/Si after spray deposition and final cleaning/drying.

utilized the passivation layer as the mask layer in device isolation. The passivation layer needs to withstand the plasma oxygen etching of the CNTs to be suitable as a masking layer.

In this paper, we report high-performance carbon nanotube field effect transistor (CNTFET) arrays fabricated via a new facile nonlithographic fabrication method that employs spray-coating of the nanotubes, evaporation of hafnium oxide (HfO_2), and then shadow mask patterning of HfO_2 to form a passivation layer over the channel (Figure 1). The passivation layer protects the nanotubes in the active channels during device isolation etching and also insulates them from the environment in subsequent use (Figure 1, Step 3). 99% pure semiconducting SWCNTs were first deposited on the substrate by spraying (here, we employed two Si-based substrates, HfO_2/Si and SiO_2/Si). Two complementary shadow masks were used sequentially to first pattern Ti/Au electrodes and then to pattern a protective HfO_2 passivation layer prior to device isolation by plasma etching. The use of shadow mask patterning techniques, which has not previously been reported in SWCNT-based FET fabrication, avoids the above-mentioned contamination and size-limitation problems of photolithography. With proper HfO_2 deposition technique conditions, the p-type semiconducting behavior of the *s*-SWCNTs is preserved. The relationships between mobility, on/off ratio, and channel length of various SWCNT devices fabricated on SiO_2 and HfO_2 gate dielectrics with different channel lengths (L = 90−180 μm for the former, L = 60−120 μm for the latter) were analyzed. Most of the devices fabricated for this report have mobilities greater than 10 $cm^2/(V\ s)$. With HfO_2 dielectric, the devices can achieve mobility of 46 $cm^2/(V\ s)$ and on/off ratio of 1×10^4. After 300 days, the device performance does not deteriorate. This technique is readily scalable to mass fabrication of CNTFETs.

EXPERIMENTAL SECTION

Wafer Substrate Preparations. CNTFETs were fabricated on silicon with either silicon dioxide (300 nm) or hafnium dioxide (42 nm) as gate dielectric layer. The SiO_2/Si was cleaned in piranha solution (H_2SO_4 and H_2O_2 in 3:1 ratio) at 120 °C for 30 min, rinsed thoroughly with deionized water, and air-dried.

For devices with HfO_2 dielectric, the Si substrate was first plasma-cleaned with oxygen plasma at 100W RF power for 2 min. Then 30 nm of HfO_2 film was deposited by E-beam evaporation at the rate of 0.03 nm/s with base pressure of 3×10^{-6} mbar. The thickness was monitored with a quartz crystal thickness monitor inside the processing chamber. A second, pinhole-free, layer of HfO_2 of 12 nm thickness was deposited on the first HfO_2 layer by atomic layer deposition method. A commercial ALD reactor (Cambridge Nanotech Inc., Savannah 100) was used for the second HfO_2 layer deposition. The precursor used for film deposition was Tetrakis(dimethylamido)-Hafnium ($Hf(NMe_2)_4$). Water and $Hf(NMe_2)_4$ were introduced alternatively at 60 s intervals over 120 cycles. The dose times were 15 ms for water and 150 ms for the precursor. During deposition, nitrogen flow was fixed at 20 sccm and chamber temperature was kept at 120 °C. The ALD process recipe was set with a low deposition rate of ∼1 Å/cycle in order to achieve high quality and pinhole free dielectric film. Each process cycle needs 2 min to complete. Hence we used e-beam to deposit first 30 nm of HfO_2 and then used ALD to deposit the second layer of 12 nm pinhole free HfO_2. After deposition of the gate dielectric, the HfO_2/Si substrate was also cleaned in piranha solution (H_2SO_4 and H_2O_2 in 3:1 ratio) at 120 °C for 30 min, rinsed thoroughly with deionized water and air-dried.

Device Preparation. Both substrates (SiO_2/Si and HfO_2/Si) were treated with 0.5 vol% aminopropyltriethoxysilane (APTES) in methanol for 1 h and then rinsed with methanol and air-dried. The CNT solution used in the spraying process was made from purified 99% semiconducting (original concentration 0.01 mg/mL) nanotubes from Nanointegris Inc. The solution was further diluted with DI water to 0.0005 mg/mL concentration. The diluted solution was then ultrasonicated at room temperature for 10 min. Semiconducting carbon nanotube network films were fabricated by spray coating the well-dispersed solution onto the substrate (Step 1, Figure 1). The spray deposition technique for preparing carbon nanotube film on substrate is ideal because of low cost, ease of use, and suitability for scale manufacturing.[39] In this technique, CNT solution is atomized from an air brush nozzle and deposited on a heated substrate to produce a CNT network film with a uniform distribution of nanotubes. During the CNT spraying process, the substrates were kept at elevated temperature, ∼100 °C, on a hot plate to promote solvent evaporation and prevent solvent buildup and CNT flow over

the substrate ("coffee-ring effect"). To prevent buildup of surfactant and other contamination, the spraying was interrupted after each 1 mL of CNT solution and the partially CNT-coated substrates were rinsed with deionized water and air-dried. Figure 1 schematically illustrates the fabrication procedure. A final cleaning/drying of the substrate was done after completion of the spraying process. After the CNT deposition and final cleaning, the samples were annealed at 100 °C in ambient air for 2 h to remove moisture. Source (S) & drain (D) electrodes made of Ti (5 nm)/Au(50 nm) were patterned with the first shadow mask pattern by electron-beam evaporation (Step 2, Figure 1). After the electrode deposition, a 50 nm layer of HfO_2 was deposited on the channel regions by E-beam through the second shadow mask pattern (Step 3, Figure 1). After depositing the protective passivation layer on the device channels, carbon nanotubes on other areas of the substrate were removed by oxygen plasma etching (Step 4, Figure 1).

Characterizations. AFM images of the samples after spray deposition and final cleaning/drying were performed with a MFP 3D microscope (Asylum Research) in AC mode to check the tube density at different positions on the substrate. Electrical parameter measurements were performed with a Keithley semiconductor parameter analyzer, model 4200-SCS. Extracted parameters were analyzed to evaluate the performance of the devices. All devices were fabricated with back gate configuration, with channel width of 50 μm and channel lengths ranging from 60 to 180 μm. Transfer characteristics were measured at V_{ds} = 2 V for devices fabricated on SiO_2 gate dielectric and at V_{ds} = 0.5 V for devices on HfO_2 gate dielectric. The on-current for devices on SiO_2/Si substrate is defined herein to be the measured value of drain current at gate voltage −40 V and drain voltage 2 V, and for HfO_2/Si substrate at gate voltage −2 V and drain voltage 0.5 V. All the devices show p-type field effect characteristics. We used the forward sweep (gate voltage sweep starts from positive to negative) of the transfer characteristics for all mobility calculations. The mobility was calculated from the standard equation $\mu_{ef\,f} = (L_C/W_C)(1/C_{ox})(1/V_d)(\partial I_d/\partial V_g)$ where L_C is the channel length, W_C is the channel width, V_d is the source−drain bias, and C_{ox} is the capacitance per unit area between gate and nanotube network. C_{ox} was estimated using the standard parallel plate model, which treats the nanotube network as a uniform film.

RESULTS AND DISCUSSION

Figure 2 shows representative AFM images of SWCNTs deposited on heated HfO_2/Si and SiO_2/Si substrates by the spraying method (after Step 1, Figure 1). The nanotubes appear to be uniformly distributed. Proper substrate surface treatment and spraying process parameters are essential for high areal density and uniform distribution of the SWCNTs. The substrate surfaces have been functionalized with amino-silane, which is known to enhance the uniform adsorption of nanotubes and to improve the performance of nanotube thin film transistors.[40] Heating the substrate to about the boiling point of the CNT carrier solvent, in this case water, improves the network uniformity as it promotes rapid evaporation of the solvent, thereby preventing solvent accumulation and CNT flow over the substrate.

Figure 3a shows images of the resulting device arrays. The gate dielectrics of devices on SiO_2/Si and HfO_2/Si substrates are 300 and 42 nm thick, respectively. Panels b and c in Figure 3 show a representative SiO_2/Si device before and after the etching of unmasked CNTs to isolate the individual devices. Comparison of Figures 3b-ii and 3c-ii shows that the CNTs surrounding the device were completely removed by the O_2 plasma etching. O_2 plasma, which is much more reactive with CNTs than it is with HfO_2, readily ashes the nanotubes to CO_2 so that the HfO_2 on the device channel acts both as etch mask and as a passivation layer.

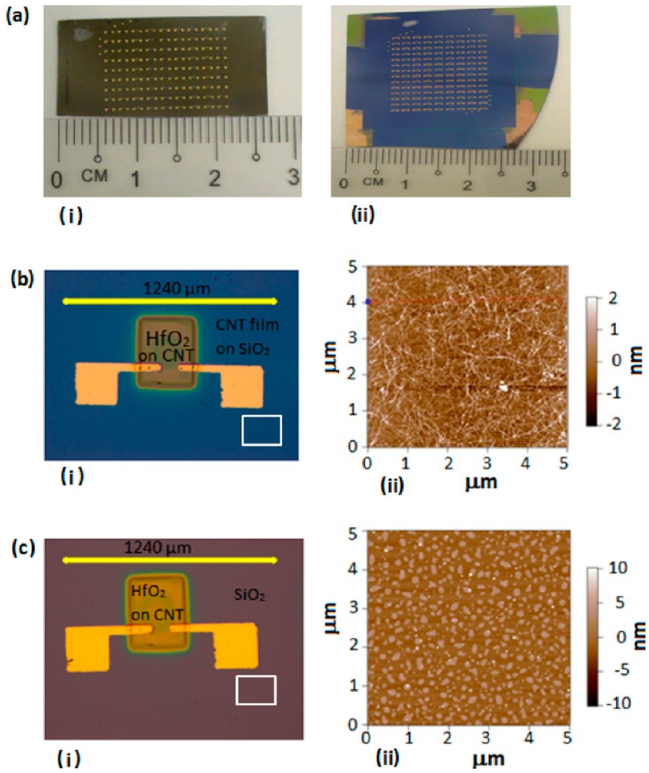


Figure 3. (a) Arrays of passivated devices fabricated on (i) HfO_2/Si and (ii) SiO_2/Si substrate. (b) a FET on SiO_2/Si substrate prior to isolation etch: (i) optical micrograph, (ii) AFM image of unetched unprotected nanotubes in the indicated region of i; (c) the same FET after isolation etch (i) optical micrograph, (ii) AFM image of same region as b, (ii) after isolation etch.

Panels a and b in Figure 4 show the transfer characteristics of typical HfO_2 covered devices on SiO_2/Si and HfO_2/Si substrates. The mobilities of the SiO_2/Si and HfO_2/Si devices are both high (9 $cm^2/(V\,s)$ and 30 $cm^2/(V\,s)$, respectively) and the on/off ratios of the devices are also both high, about 1×10^4. The networks are dense enough to have good connectivity while the washing cycle during the spray deposition process reduces intertube and tube/electrode contact resistance, leading to the observed high on-currents, which are in the microampere range.

Others have reported that passivation with HfO_2 by the atomic layer deposition (ALD) technique changes the CNT-based FET behavior from p-type to n-type.[8,34] However, our devices exhibit characteristics of p-type CNTFETs, even with the HfO_2 passivating layer deposited by E-beam deposition (Figure 4). They have no n-type behavior and are in the off state under positive gate voltage. During our deposition of the HfO_2 passivation layer, we flowed pure oxygen through the chamber in order to preserve adsorbed oxygen on the active channel. The interaction of adsorbed oxygen and the work function of the contact metal (i.e., Au) affects the device behavior. With adsorbed oxygen on the channel CNTs, negative charge stored near the source and drain contacts in the channel bends the energy band up and reduces the Schottky barrier height for holes. When a negative gate voltage is applied to the device, the energy band bends up more resulting in further reduction in barrier height which causes the holes to tunnel through and the transistor to turn on (see the Supporting Information, Figure S1). With higher positive gate

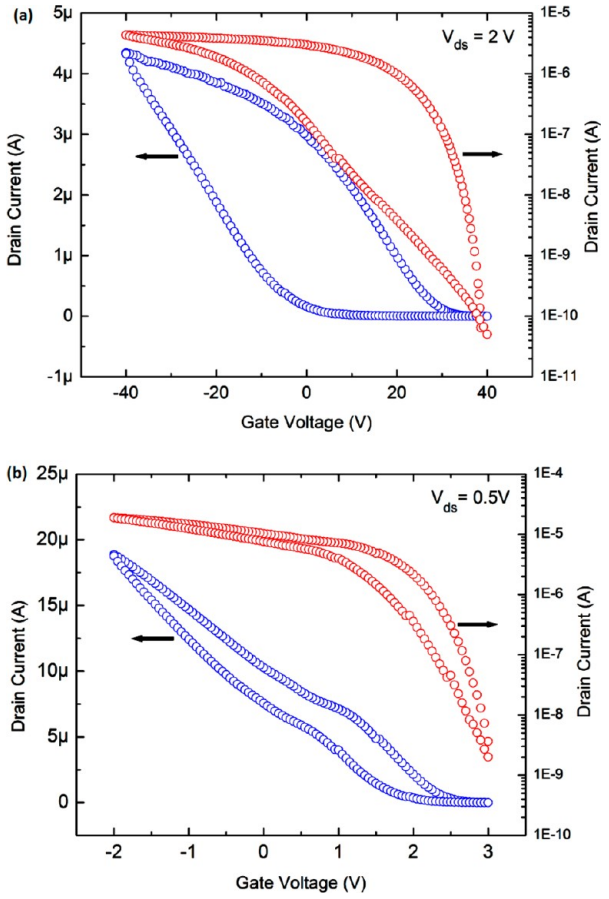


Figure 4. Typical transfer characteristic (drain current I_d vs gate voltage V_g) of a covered channel device on (a) SiO_2/Si substrate (channel length 120 μm) and (b) HfO_2/Si substrate (channel length 60 μm), exhibiting semiconducting behavior with on/off ratio $\geq 1 \times 10^4$.

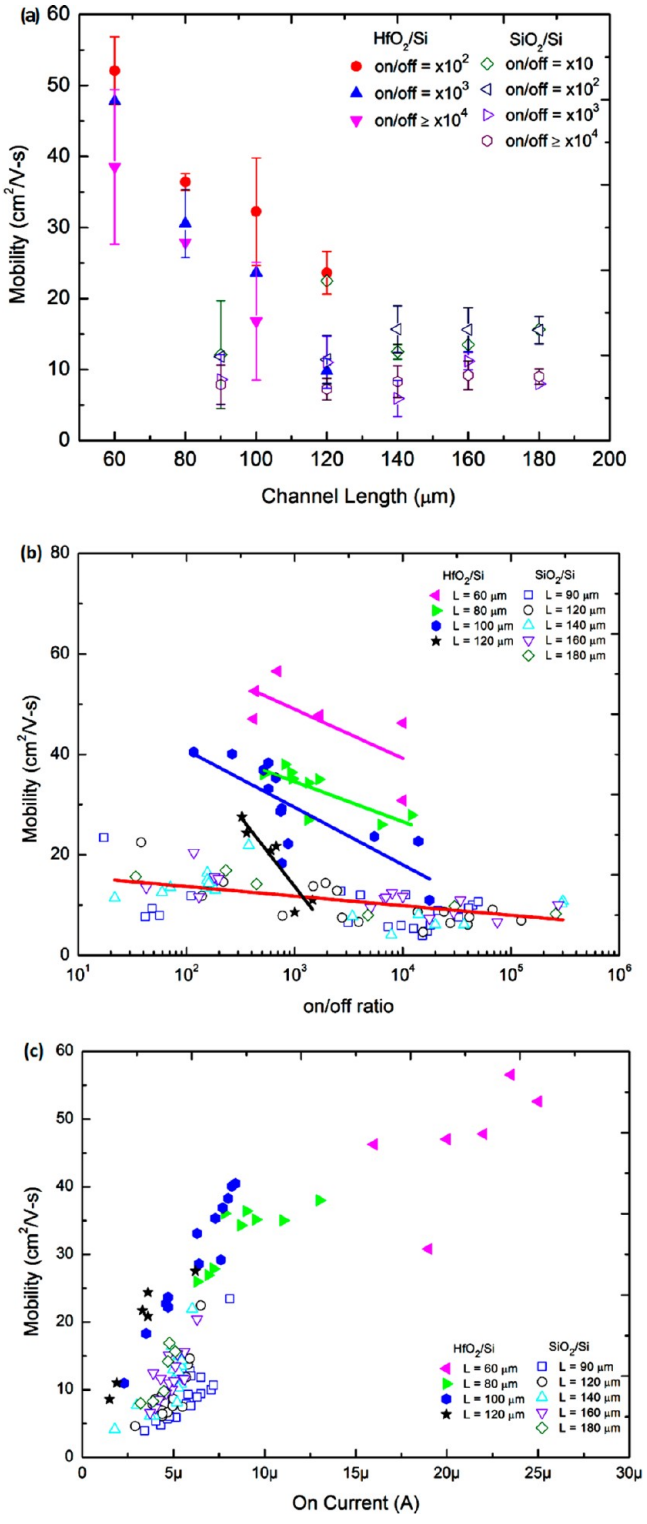


Figure 5. Correlations of electronic properties with each other and with channel length for transistors fabricated on SiO_2/Si and HfO_2/Si substrates. On current for SiO_2/Si substrate devices was measured with $V_g = -40$ V, $V_{ds} = 2$ V; for HfO_2/Si substrate devices, with $V_g = -2$ V, $V_{ds} = 0.5$ V. (a) Mobility versus channel length of transistors grouped by on/off ratio. (b) Mobility versus on/off ratio. The indicated channel lengths ("L") are in micrometers. (c) Mobility versus on-current.

voltage, the barrier height for holes increases and device will be off. Hence in the presence of oxygen, CNT devices with Au contacts in ambient conditions show p-type transistor behavior.

Figure 4 also shows that the passivated HfO_2/Si device (bottom figure) has smaller hysteresis than the passivated SiO_2/Si substrate device (top figure). Gate hysteresis of CNTFETs must be controlled to a modest level for most electronic applications. Hysteresis in CNTFETs is mostly due to charge trapping from water molecules adsorbed on the carbon nanotubes.[41] At ambient conditions, the SiO_2 surface has Si−OH silanol groups that are susceptible to hydration by water molecules because of hydrogen bonding. For HfO_2/Si substrate devices, the hysteresis will be less as HfO_2 is less hydrophilic and is less hydrated. The ratio of normalized hysteresis for SiO_2 and HfO_2 gate dielectric devices, by considering the dielectric constants of SiO_2 and HfO_2 is ∼1.1 indicates that the normalized hysteresis is almost same for SiO_2 and HfO_2 gate dielectric devices.[42] (Transfer characteristics of the device at different drain voltages are given in the Supporting Information, Figure S2).

Electrical characterizations were performed for various SiO_2/Si and HfO_2/Si devices with varying channel lengths (L = 90−180 μm for SiO_2/Si and L = 60−120 μm for HfO_2/Si) and the on/off ratio and carrier mobility parameters were extracted. The channel length dependence of mobility for devices with different on−off ratios is shown in Figure 5a. For practical transistors, the on/off ratio should be about 1×10^4 or more. For HfO_2/Si devices, the general behavior is a decrease of

dx.doi.org/10.1021/am302431e | ACS Appl. Mater. Interfaces 2012, 4, 7047−7054

mobility with increase in channel length. Among the high on/off ($\sim 1 \times 10^4$) devices, the one with the highest mobility (46) is a short-channel (60 μm) device. These values are higher than many other previously reported values.[43−45] Normally shorter channel length devices have fewer tube to tube junctions and, consequently, high mobility. Also for lower channel length devices, the effective field at the source/CNT contact will be higher, because of constant drain−source voltage, which effectively reduces the Schottky barrier height and increases the drive current and mobility.[46,47] For the SiO_2/Si devices investigated here, the channel lengths are longer, and the mobilities are rather invariant with respect to channel length variation. With SiO_2/Si devices, the mobilities can reach 12 $cm^2/(V\ s)$ with an on/off ratio of 1×10^4.

Figure 5b shows scatterplots and trend lines of mobility versus on/off ratio of individual devices for all devices fabricated in this study. Figure 5b suggests that straight lines are reasonable regressions, implying that in these devices the on/off ratio is proportional to exp(−mobility/λ), where λ is the slope. For both dielectrics, the mobility is anticorrelated with on/off ratio. This is attributable to the differing character of the effects of variation in SWNT network density on (1) the on-current and mobility of the high-density semiconducting network and (2) the off-current through the much lower density metallic network. The sparse metallic network is much more percolation limited than the dense semiconducting network and so its current capacity is much more sensitive to device-to-device variation in network density than is the on-current and mobility of the semiconducting network. Both off-current and on-current/mobility increase with increasing network density, but the off-current increases proportionately much more. Device-to-device network density variations interact with these differing sensitivities to produce the observed anticorrelation. When the metallic network is much sparser than the semiconducting network, this anticorrelation is inevitable.

Devices fabricated on HfO_2/Si substrate generally have higher mobility than SiO_2/Si devices (Figure 5b). The higher dielectric constant of HfO_2 (12 compared to 3.9 for SiO_2) results in higher capacitance which lowers the gate voltage and increases the transconductance, $\partial I_d/\partial V_g$, so as to enhance device mobility.[48,49] HfO_2 devices have transconductances of about 5 μA/V (Figure 4b) compared to $\sim$0.1 μA/V for SiO_2 devices. The thickness of SiO_2 gate dielectric is 300 nm and HfO_2 gate dielectric is 42 nm. For thin HfO_2 gate dielectric, smaller gate voltage is needed to turn on the device compared to larger gate voltage for thick SiO_2 gate dielectric. In mobility calculation, the parameters such as transconductance, gate capacitance and drain−source voltage etc are included. In our thin HfO_2 gate dielectric device, the drain-source voltage is 0.5 V compared to 2 V applied for the thick SiO_2 gate dielectric device. The transconductance versus gate bias of a typical device with HfO_2 gate and SiO2 gate dielectric is presented in the Supporting Information, Figure S3. The transconductance for the HfO_2 gate device is 6 μS and for SiO2 device is 0.12 μS. The combined effect of larger transconductance and smaller drain-source voltage attributes to higher mobility of the HfO_2 devices. The HfO_2 devices have mobilities that are multiples of the SiO_2 device mobilities. A unique advantage of carbon nanotubes is their compatibility with high-k dielectrics such as HfO_2. The lack of dangling bonds at the CNT/HfO_2 interfaces and the weak noncovalent bonding interactions between CNTs and HfO_2 prevent charge losses and improve the device mobility.[15,50]

Figure 5c shows that the mobility varies linearly with on-current (except for the shortest channel length of 60 μm). As the semiconducting network is nearly continuous, we expect the on-current to vary linearly with nanotube density in the channel. These correlations suggest that on/off ratio is roughly proportional to exp(−network density/Λ), where Λ is the slope. The metallic network density is about 1% of that of the semiconducting network and is percolation limited, so that the current capacity of the metallic network is highly sensitive to fabrication variation in total nanotube density in the channel.

Figure 5c shows the variation with on-current of mobility for different devices (a population of different devices at each of the channel lengths). For the HfO_2/Si devices, at a fixed channel length, the on-current varies over a significant range. For example, for L = 60 μm, the on-current (in microamperes) varies from 16 (min) to 25 (max). The mobilities of most devices, except the shortest channel length (60 μm) devices, increase almost linearly with increasing on-currents and fall approximately on a straight line. The linear relationship is due to the common dependence of both the conductance and the transconductance on variations in the underlying channel network density and CNT properties. The scatter in each fixed channel length population is due to fabrication variation in channel network density. Both on-current and mobility vary in the same way with respect to this fabrication variability of the channel density to produce the observed linear correlation of on-current and mobility. Use of a more mechanized air gun in the CNT spray process could greatly reduce the network density variability and tighten the distribution of fabricated device properties. Comparison in Figure 5c of HfO_2/Si with SiO_2/Si devices of the same or similar channel length indicates that the two sets of devices have similar on currents (of 2.5−12.5 μA) at comparable channel length but the HfO_2/Si devices have significantly higher mobility.

Wang et al. reported decrease of on-current density with increase in channel length for fabricated devices using separated nanotubes.[31] The mobility of their devices also decreases with increase in channel length. They explained that the device mobility is limited by the percolative transport through nanotube network. As the channel length is much larger than the tube length, there will be more intertube junctions so that mobility decreases with increasing channel length. Similar behavior of decrease in current density with increase in channel length was also reported by Rouhi et al. and Liyanage et al.[30,32] In the case of Rouhi's work, even though on-current decreases with increase in channel length, the mobility shows an increase with increase in channel length. They attributed the increase in mobility with longer channel length device to be due to higher tube density, which it appears was not kept constant. For our devices on HfO_2/Si substrate with fixed on−off ratio, the mobility is higher for shorter channel length devices (Figure 5a). This is consistent with Wang's et al. model that mobility decreases with increasing channel length. We also observed that with HfO_2/Si substrate (Figure 5b), for fixed channel length, the on−off ratio is strongly anticorrelated with mobility, which is, as we have previously noted, due to the strong dependence of the off-current on the density of the sparse metallic network in the channel.

The reliability and predictability of CNTFET performance is important for electronics applications. To study the long-term stability and reliability of the passivated devices, the devices

were exposed to ambient conditions for more than 300 days and their electrical properties were remeasured. Figure 6 shows

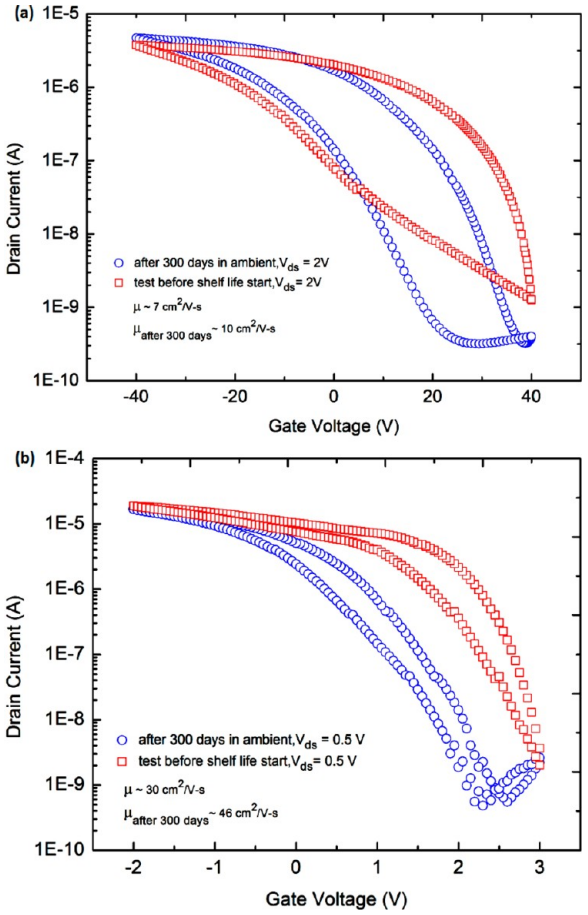


Figure 6. I_d–V_g plot of a device on (a) SiO_2/Si and (b) HfO_2/Si substrate immediately after fabrication and after 300 days of exposure to ambient conditions.

the transfer characteristics of a typical device fabricated on SiO_2/Si and HfO_2/Si substrates just after fabrication and also after 300 days of exposure to ambient conditions. The device performance did not degrade after this lengthy exposure. The mobility of the SiO_2 dielectric device after 300 days remains high at 10 $cm^2/(V\ s)$ with on/off ratio of order 1×10^4 (the on/off ratio actually increases somewhat). The mobility of HfO_2 gate dielectric device after 300 days also remains high at 46 $cm^2/(V\ s)$ with on/off ratio of order 1×10^4. Protection of the CNT channel with HfO_2 thin film reduces the effects of environmental insults to the active channel during prolonged exposure to and operation in ambient conditions.

CONCLUSIONS

In conclusion, we have fabricated high-performance CNTFET devices with a nonlithographic method involving shadow masking to achieve both channel passivation and device isolation with HfO_2. The patterned HfO_2 effectively acts as a mask for removal of unwanted nanotubes outside the channels and also protects the channel nanotubes from the environment during subsequent device operation. Most of the fabricated devices have mobility $\geq$10 $cm^2/(V\ s)$. The best performing device on HfO_2/Si substrate with channel length of 60 μm has mobility of 46 $cm^2/(V\ s)$ with on/off ratio of order 10^4. This work demonstrates the feasibility and utility of inexpensive shadow mask technology in the fabrication of high performance CNTFET devices. This method avoids the use of expensive and contaminating lithography processes, which also reduces the production cost. Because the device fabrication process involves protection of the active channel with a covering of HfO_2, long-term environmental stability of the fabricated devices can be achieved.

ASSOCIATED CONTENT

Supporting Information

Transfer characteristics of the device at different drain voltages and transconductance of the device versus gate bias (PDF). This material is available free of charge via the Internet at http://pubs.acs.org/.

AUTHOR INFORMATION

Corresponding Author

*E-mail: MBEChan@ntu.edu.sg.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This work was supported by a Competitive Research Program grant from the Singapore National Research Foundation (NRF-CRP2-2007-02).

REFERENCES

(1) Rogers, J. A.; Someya, T.; Huang, Y. G. *Science* **2010**, *327*, 1603–1607.
(2) Liu, X.; Long, Y. Z.; Liao, L.; Duan, X. F.; Fan, Z. Y. *ACS Nano* **2012**, *6*, 1888–1900.
(3) Fan, Z. Y.; Ho, J. C.; Takahashi, T.; Yerushalmi, R.; Takei, K.; Ford, A. C.; Chueh, Y. L.; Javey, A. *Adv. Mater.* **2009**, *21*, 3730–3743.
(4) Long, Y. Z.; Yu, M.; Sun, B.; Gu, C. Z.; Fan, Z. Y. *Chem. Soc. Rev.* **2012**, *41*, 4560–4580.
(5) Thanh, Q. N.; Jeong, H.; Kim, J.; Kevek, J. W.; Ahn, Y. H.; Lee, S.; Minot, E. D.; Park, J. Y. *Adv. Mater.* **2012**, *24*, 4499–4504.
(6) Cao, Q.; Kim, H. S.; Pimparkar, N.; Kulkarni, J. P.; Wang, C. J.; Shim, M.; Roy, K.; Alam, M. A.; Rogers, J. A. *Nature* **2008**, *454*, 495–U494.
(7) Sun, D. M.; Timmermans, M. Y.; Tian, Y.; Nasibulin, A. G.; Kauppinen, E. I.; Kishimoto, S.; Mizutani, T.; Ohno, Y. *Nat. Nanotechnol.* **2011**, *6*, 156–161.
(8) Zhang, J. L.; Wang, C.; Fu, Y.; He, Y. C.; Zhou, C. W. *ACS Nano* **2011**, *5*, 3284–3292.
(9) Bachtold, A.; Hadley, P.; Nakanishi, T.; Dekker, C. *Science* **2001**, *294*, 1317–1320.
(10) Lee, S. Y.; Lee, S. W.; Kim, S. M.; Yu, W. J.; Jo, Y. W.; Lee, Y. H. *ACS Nano* **2011**, *5*, 2369–2375.
(11) Cao, Q.; Rogers, J. A. *Adv. Mater.* **2009**, *21*, 29–53.
(12) Wang, C. A.; Zhang, J. L.; Zhou, C. W. *ACS Nano* **2010**, *4*, 7123–7132.
(13) Avouris, P.; Martel, R.; Derycke, V.; Appenzeller, J. *Phys. B: Condens. Matter* **2002**, *323*, 6–14.
(14) Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. J. *Nature* **2003**, *424*, 654–657.
(15) Dai, H. J.; Javey, A.; Pop, E.; Mann, D.; Kim, W.; Lu, Y. R. *Nano* **2006**, *1*, 1–13.
(16) Beecher, P.; Servati, P.; Rozhin, A.; Colli, A.; Scardaci, V.; Pisana, S.; Hasan, T.; Flewitt, A. J.; Robertson, J.; Hsieh, G. W.; Li, F. M.; Nathan, A.; Ferrari, A. C.; Milne, W. I. *J. Appl. Phys.* **2007**, *102*, 043710.
(17) Okimoto, H.; Takenobu, T.; Yanagi, K.; Miyata, Y.; Shimotani, H.; Kataura, H.; Iwasa, Y. *Adv. Mater.* **2010**, *22*, 3981–3986.
(18) Liu, J.; Hersam, M. C. *MRS Bull.* **2010**, *35*, 315–321.

(19) Liu, H. P.; Nishide, D.; Tanaka, T.; Kataura, H. *Nat. Commun* **2011**, *2*, 309.
(20) Hersam, M. C. *Nat. Nanotechnol.* **2008**, *3*, 387−394.
(21) Bonaccorso, F.; Hasan, T.; Tan, P. H.; Sciascia, C.; Privitera, G.; Di Marco, G.; Gucciardi, P. G.; Ferrari, A. C. *J. Phys. Chem. C* **2010**, *114*, 17267−17285.
(22) Antaris, A. L.; Seo, J. W. T.; Green, A. A.; Hersam, M. C. *ACS Nano* **2010**, *4*, 4725−4732.
(23) Wang, W. Z.; Li, W. F.; Pan, X. Y.; Li, C. M.; Li, L. J.; Mu, Y. G.; Rogers, J. A.; Chan-Park, M. B. *Adv. Funct. Mater.* **2011**, *21*, 1643−1651.
(24) Chattopadhyay, D.; Galeska, L.; Papadimitrakopoulos, F. *J. Am. Chem. Soc.* **2003**, *125*, 3370−3375.
(25) Krupke, R.; Hennrich, F.; von Lohneysen, H.; Kappes, M. M. *Science* **2003**, *301*, 344−347.
(26) LeMieux, M. C.; Sok, S.; Roberts, M. E.; Opatkiewicz, J. P.; Liu, D.; Barman, S. N.; Patil, N.; Mitra, S.; Bao, Z. *ACS Nano* **2009**, *3*, 4089−4097.
(27) Miyata, Y.; Shiozawa, K.; Asada, Y.; Ohno, Y.; Kitaura, R.; Mizutani, T.; Shinohara, H. *Nano Res.* **2011**, *4*, 963−970.
(28) Ha, M. J.; Xia, Y.; Green, A. A.; Zhang, W.; Renn, M. J.; Kim, C. H.; Hersam, M. C.; Frisbie, C. D. *ACS Nano* **2010**, *4*, 4388−4395.
(29) Rouhi, N.; Jain, D.; Zand, K.; Burke, P. J. *Adv. Mater.* **2011**, *23*, 94.
(30) Rouhi, N.; Jain, D.; Burke, P. J. *ACS Nano* **2011**, *5*, 8471−8487.
(31) Wang, C.; Zhang, J. L.; Ryu, K. M.; Badmaev, A.; De Arco, L. G.; Zhou, C. W. *Nano Lett.* **2009**, *9*, 4285−4291.
(32) Liyanage, L. S.; Lee, H.; Patil, N.; Park, S.; Mitra, S.; Bao, Z. N.; Wong, H. S. P. *ACS Nano* **2012**, *6*, 451−458.
(33) Timmermans, M. Y.; Grigoras, K.; Nasibulin, A. G.; Hurskainen, V.; Franssila, S.; Ermolov, V.; Kauppinen, E. I. *Nanotechnol.* **2011**, *22*, 065303.
(34) Moriyama, N.; Ohno, Y.; Kitamura, T.; Kishimoto, S.; Mizutani, T. *Nanotechnol.* **2010**, *21*, 165201.
(35) Kaminishi, D.; Ozaki, H.; Ohno, Y.; Maehashi, K.; Inoue, K.; Matsumoto, K.; Seri, Y.; Masuda, A.; Matsumura, H. *App. Phy. Lett.* **2005**, *86*, 113115.
(36) Rispal, L.; Tschischke, T.; Yang, H.; Schwalke, U. *Jap. J. App. Phys.* **2008**, *47*, 3287−3291.
(37) Selvarasah, S.; Li, X. H.; Busnaina, A.; Dokmeci, M. R. *App. Phy. Lett.* **2010**, *97*, 153120.
(38) Franklin, A. D.; Tulevski, G. S.; Han, S. J.; Shahrjerdi, D.; Cao, Q.; Chen, H. Y.; Wong, H. S. P.; Haensch, W. *ACS Nano* **2012**, *6*, 1109−1115.
(39) Zhao, X.; Chu, B. T. T.; Ballesteros, B.; Wang, W. L.; Johnston, C.; Sykes, J. M.; Grant, P. S. *Nanotechnol.* **2009**, *20*, 065605.
(40) Opatkiewicz, J. P.; LeMieux, M. C.; Bao, Z. N. *ACS Nano* **2010**, *4*, 1167−1177.
(41) Kim, W.; Javey, A.; Vermesh, O.; Wang, O.; Li, Y. M.; Dai, H. J. *Nano Lett.* **2003**, *3*, 193−198.
(42) Jin, S. H.; Islam, A. E.; Kim, T. I.; Kim, J. H.; Alam, M. A.; Rogers, J. A. *Adv. Funct. Mater.* **2012**, *22*, 2276−2284.
(43) Lee, C. W.; Han, X. D.; Chen, F. M.; Wei, J.; Chen, Y.; Chan-Park, M. B.; Li, L. J. *Adv. Mater.* **2010**, *22*, 1278.
(44) Zhao, J. W.; Lin, C. T.; Zhang, W. J.; Xu, Y. P.; Lee, C. W.; Chan-Park, M. B.; Chen, P.; Li, L. J. *J. Phys. Chem. C* **2011**, *115*, 6975−6979.
(45) Roberts, M. E.; LeMieux, M. C.; Bao, Z. N. *ACS Nano* **2009**, *3*, 3287−3293.
(46) Appenzeller, J.; Knoch, J.; Derycke, V.; Martel, R.; Wind, S.; Avouris, P. *Phys. Rev. Lett.* **2002**, *89*, 126801.
(47) Cummings, A. W.; Leonard, F. *ACS Nano* **2012**, *6*, 4494−4499.
(48) Javey, A.; Guo, J.; Farmer, D. B.; Wang, Q.; Wang, D. W.; Gordon, R. G.; Lundstrom, M.; Dai, H. J. *Nano Lett.* **2004**, *4*, 447−450.
(49) Choi, J. H.; Mao, Y.; Chang, J. P. *Mater. Sci. Eng., R* **2011**, *72*, 97−136.
(50) Javey, A.; Kim, H.; Brink, M.; Wang, Q.; Ural, A.; Guo, J.; McIntyre, P.; McEuen, P.; Lundstrom, M.; Dai, H. J. *Nat. Mater.* **2002**, *1*, 241−246.